REMARKS

Claims 1-30 are pending. Claims 1-3, 11-13 and 21-23 are rejected. Claims 4-10, 14-20 and 24-30 are objected to.

Drawing Amendments

Applicant has enclosed a Replacement drawing sheet for Figures 3A-C, which have been amended to include the label "Prior Art."

Claim Objections

Claims 22-30 are objected to due to an informality, but have been amended to overcome the objections.

Specification

The Abstract has been amended to comply with the required word count. In addition, the disclosure has been amended to correct various informalities. No new matter has been added.

Claim Rejections - 35 U.S.C. § 102

Claims 1-3 and 21-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,544,105 issued to Hirose et al. (hereinafter "Hirose").

Applicant respectfully traverses the rejections of claims 1-3 and 21-23 under 35 U.S.C. § 102(b) as being anticipated by Hirose. Specifically, Examiner has asserted that Hirose discloses an equilibration circuit (LB) connected to the first and second bitlines. Applicant respectfully disagrees that the circuit designated by LB comprises an equilibration circuit as recited in independent claims 1, 11, and 21. Examiner cites Figures 25 and 27 and the related discussion in columns 25-27 and 29-30 as support for the proposition that Hirose teaches an equilibration circuit. Referring to column 25, line 39 of Hirose, the LB circuit is described as a bit line load circuit that is operable to precharge the bit lines "bit" and "/bit." The bit line load circuit LB, therefore, is not the equilibration circuit recited by Applicant in independent claims 1, 11 and 21. Instead the

LB circuit disclosed in Hirose is performs the prior art precharge function, described in the background of Applicant's invention.

The equilibration circuit disclosed in Applicant's invention is operable to maintain a predetermined equilibrium condition between the first and second bitlines. Furthermore, the equilibration circuit is operable to generate an impedance load in the first and second bitlines at a level that allows generation of differential signals in the bitlines. The system and method disclosed in Applicant's invention allows memory cell bitlines to move from a sensed state "low" to the opposite state "high" without an intervening precharge, thereby providing a significant increase in performance. In this regard, it is noted that the memory cells disclosed in Hirose all require precharge of the respective bitlines.

For the reasons discussed above, Applicant respectfully submits that the rejections of claims 1-3 and 21-23 under 35 U.S.C. §102(b) should be removed. Regarding the rejection of claims 11-13 under 35 U.S.C. §102(b), Examiner has stated that they encompass the same scope and invention as that of claims 1-3 and 21-23. Applicant respectfully submits, therefore, that the rejections of claims 11-13 under 35 U.S.C. §102(b) should also be removed.

CONCLUSION

In view of the amendments and remarks set forth herein, Applicant respectfully submits that all pending claims are in condition for allowance. Accordingly, Applicant requests that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on September 15, 2005.

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Respectfully submitted,

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